Amendments to the Specification:

Please amend the specification as follows:

Please replace paragraph 0067 of the published patent application 2006/0244707, with the following rewritten paragraph:

The work memory 12 includes H x V x n memory cells 12a arranged in V lines and H x n columns, H x n bit lines 12b, H x n complementary bit lines 12c, V word lines 12d, a horizontal address decoder 12e, a vertical address decoder 12f, and an output circuit 12g. The memory cells 12a are disposed at the respective intersections of the bit lines 12b and the word lines 12c. Each memory cell 12a is connected to the associated bit line 12b and complementary bit line 12c, and additionally connected to the associated word line 12d. The horizontal and ~~horizontal~~ vertical address decoders 12e and 12f are used to select the memory cells 12a to be accessed. The bitmap data 21 received from the graphic engine 11 are stored in the desired ones of the memory cells 12a. The bit lines 12b and the complementary bit lines 12c are connected to the output circuit 12g.

Please replace paragraph 0070 of the published patent application 2006/0244707, with the following rewritten paragraph:

Similarly to the work memory 12, the display memory 13 includes H x V x n memory cells 13a arranged in V lines and H x n columns, H x n bit lines 13b, H x n complementary bit lines 13c, V word lines 13d, a horizontal address decoder 13e, a vertical address decoder 13f, and an output circuit 13g. The memory cells 13a are disposed at the respective intersections of the bit lines 12b and the word lines 12c. Each of the memory cells 13a is connected to the associated bit line 13b and complementary bit line 13c, and additionally connected to the associated word line 13d. The horizontal and ~~horizontal~~ vertical address decoders 13e and 13f are used to select the memory cells 13a to be accessed in response to the control signal 23 received from the memory control circuit 18. The bit lines 13b and the complementary bit lines 13c are connected to the output circuit 13g. The output circuit 13g is designed to output the pixel data associated with the desired pixel line at the same time.